WHAT IS CLAIMED IS:

1. An evaluation method of a TFT characterized by

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode over a semiconductor film which is formed to have a low concentration impurity region overlapping the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and

estimating an impurity concentration of the low concentration impurity region of the TFT by the resistance.

2. An evaluation method of a TFT characterized by

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode that is laminated with a first conductive film and a second conductive film over a semiconductor film which has a low concentration impurity region overlapping the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and

estimating an impurity concentration of the low concentration impurity region of the TFT by the resistance

wherein an edge of the first conductive film extends over an edge of the second conductive film,

wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

3. The evaluation method of the TFT according to Claim 2, characterized in that the first conductive film is formed from a TaN film and the second conductive film is formed from a W

film.

4. An evaluation method of a TFT characterized by

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode with a taper over a semiconductor film which is formed to have a low concentration impurity region overlapping the taper of the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and

estimating an impurity concentration of the low concentration impurity region of the TFT in accordance with the taper by the resistance.

5. An evaluation method of a TFT characterized by

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode that is laminated with a first conductive film and a second conductive film each having a taper over a semiconductor film which has a low concentration impurity region overlapping the taper of the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and

estimating an impurity concentration of the low concentration impurity region of the TFT in accordance with the taper by the resistance,

wherein an edge of the first conductive film extends over an edge of the second conductive film,

wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

6. The evaluation method of the TFT according to Claim 5, characterized in that the first

conductive film having the taper is formed from a TaN film and the second conductive film having the taper is formed from a W film.

7. An evaluation method of a TFT characterized by

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode that is laminated with a first conductive film and a second conductive film over a semiconductor film

a step of measuring resistance of the low concentration impurity of the first TEG;

a step of measuring resistance of the channel forming region of the second TEG;

a step of measuring resistance of the impurity region of the third TEG;

estimating impurity concentrations of the low concentration impurity region, the channel forming region and the impurity region in the TFT by the resistance,

wherein the TEG includes the first TEG formed to be provided a side edge portion of the semiconductor film between an edge of the first conductive film and an edge of the second conductive film,

wherein the second TEG formed to be extended an edge of the second conductive film over a side edge portion of the semiconductor film,

wherein the third TEG formed not to be extended an edge of the first conductive film over a side edge portion of the semiconductor film,

8. The evaluation method of the TFT according to Claim 7, characterized in that a plurality of the first to the third TEGs are provided.

9. The evaluation method of the TFT according to Claim 7, characterized in that the first conductive film is formed from a TaN film and the second conductive film is formed from a W film.

10. The evaluation method of the TFT according to Claim 7, characterized in that edges of the first conductive film and the second conductive film have a taper.

11. The evaluation method of the TFT according to Claim 1, characterized in that in the TEG, a correlation of the resistance and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

12. The evaluation method of the TFT according to Claim 2, characterized in that in the TEG, a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

13. The evaluation method of the TFT according to Claim 4, characterized in that in the TEG, a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

14. The evaluation method of the TFT according to Claim 5, characterized in that a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

15. The evaluation method of the TFT according to Claim 7, characterized in that a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

16. The evaluation method of the TFT according to Claim 1, characterized in that the TEG has a test element for measuring resistance of a low concentration impurity region.

17. The evaluation method of the TFT according to Claim 2, characterized in that the TEG has a test element for measuring resistance of a low concentration impurity region.

18. The evaluation method of the TFT according to Claim 4, characterized in that the TEG has a test element for measuring resistance of a low concentration impurity region.

19. The evaluation method of the TFT according to Claim 5, characterized in that the TEG has a test element for measuring resistance of a low concentration impurity region.

20. The evaluation method of the TFT according to Claim 7, characterized in that the TEG has a test element for measuring resistance of a low concentration impurity region.

21. A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 1.

22. A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 2.

23. A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 4.

24. A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 5.

25. A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 7.

26. A method of manufacturing a semiconductor device including a TFT including a semiconductor film having an impurity region formed over an insulating substrate, and a gate electrode formed over the semiconductor film by using a mask, characterized by

forming a TEG having impurity regions in a plurality of regions on the insulating substrate,

calculating misalignment of a mask of the TEG before and/or after an activation step of the TFT, and

calculating shrinkage or expansion of the substrate by the calculated misalignment of the mask.

27. A method of manufacturing a semiconductor device including a TFT including a semiconductor film having a low concentration impurity region and a high concentration impurity region formed over an insulating substrate, and a gate electrode formed over the semiconductor film by using a mask so as to overlap the low concentration impurity region, characterized by

forming a TEG having a low concentration impurity region and a high concentration impurity region in a plurality of regions on the insulating substrate,

calculating misalignment of a mask of the TEG before and/or after an activation step of the TFT, and

calculating shrinkage or expansion of the substrate by the calculated misalignment of the mask.

28. An article characterized in

that a TEG and a TFT over a same substrate, having a gate electrode over a semiconductor film which is formed so as to have a low concentration impurity region overlapping the gate electrode.

29. An article characterized in

that a TEG and a TFT over a same substrate, having a gate electrode laminated with a first conductive film and a second conductive film over a semiconductor film which has a low concentration impurity region overlapping the gate electrode,

wherein an edge of the first conductive film extends over an edge of the second conductive film,

wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

30. The article according to Claim 29, characterized in that the first conductive film is formed from a TaN film and the second conductive film is formed from a W film.

31. The article according to Claim 28 characterized by including a gate electrode having a taper over a semiconductor film which has a low concentration impurity region overlapping the gate electrode.

32. The article according to Claim 29 characterized by including a gate electrode having a taper over a semiconductor film which has a low concentration impurity region overlapping the gate electrode.

33. A program for controlling a dosage for operating a computer that controls a quantity of impurities to be added of a TFT provided over a same substrate as a TEG

as operation means for obtaining a resistance distribution of the TEG,

as means for memorizing a manufacturing condition of a TFT or a design condition of a device,

as means for judging an quantity of impurities to be added based on the means for memorizing, and

as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.

34. A program for controlling a dosage for operating a computer that controls a quantity of impurities to be added of a TFT that has a gate electrode formed by using a mask and that is provided over a same substrate as a TEG

as operation means for obtaining a resistance distribution of the TEG by making operation of a misalignment of the mask,

as means for memorizing a manufacturing condition of a TFT or a design condition of a device,

as means for judging an quantity of impurities to be added based on the means for memorizing, and

as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.

35. A computer-readable recording medium that records a program for controlling dosage for operating a computer that controls a quantity of impurities to be added of a TFT provided over a same substrate as a TEG

as operation means for obtaining a resistance distribution of the TEG,

as means for memorizing a manufacturing condition of a TFT or a design condition of a device,

as means for judging an quantity of impurities to be added based on the means for memorizing, and

as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.

36. A computer-readable recording medium that records a program for controlling dosage for operating a computer that controls a quantity of impurities to be added of a TFT that has a gate electrode formed by using a mask and that is provided over a same substrate as a TEG

as operation means for obtaining a resistance distribution of the TEG by making operation of a misalignment of the mask,

as means for memorizing a manufacturing condition of a TFT or a design condition of a device,

as means for judging an quantity of impurities to be added based on the means for memorizing, and

as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.